INSTRUCTION MANUAL

MODEL 9200-602

TIME CODE TRANSLATOR

DATUM

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SECTION I

SYSTEM DESCRIPTION

1.1 The Model 9200 TIME CODE READER is designed to read the recorded time when played back from a magnetic tape. The unit will accept the standard IRIG B Format. By using the standard IRIG Format B, the reader is usable in conjunction with other systems or projects. The unit automatically decodes the serial input code and provides a front panel display, serial pulse trains and optional digital outputs. Reading accuracy is better than 50 microseconds when reading in the forward playback mode.

A synchronization mode, selectable from the front panel, provides noise rejection. This feature allows the selection of "zero," "three" or "infinite" time frames bypass is digital errors are detected. This feature is most important when digital outputs are required, or tape search operation is desired. With "zero" selected each time frame is read. With "three" selected, the unit is resynchronized only after three consecutive error frames. With "infinite" selected, the unit updates from the carrier only and disregards the coded information.

1.2 PHYSICAL

The Model 9200 is constructed in a slim 1-3/4" package requiring minimum 19" rack mounting or offering easy handling for desk mounting. A decimal display, located on the front panel, shows either generated time or translated time depending on mode of operation. All operating mode controls are mounted on the front panel. Each display digit is individually presettable with a single thumbwheel switch and a pushbutton for each digit. Lighted pushbuttons give a direct reading of mode.

The circuitry of the Model 9200 consists of TTL and DTL type integrated circuits. Each element is mounted in a modular socket for ultimate ease in maintainability.

SECTION II
SPECIFICATIONS

2.1 INPUTS

2.1.1 J6 POWER

(a) 115/230 VAC ±10%

(b) 48 to 420 Hz

2.1.2 J1 CODE INPUT

a. Format: IRIG B standard or modified to remove 17-bit binary STOD.

b. Modulation Frequency: 1 kHz.

c. Modulation Ratio: 6:1 - 2:1

d. Amplitude: 100 MV p-p to 10V p-p on the mark pulse.

e. Input Z: > 90K at 1 kHz.

f. Frequency Range: 25 Hz - 300 kHz.

g. Synchronization Accuracy: Less than ±50 microseconds.

2.1.3 External Translator Control Inputs - J5

a. GO: Logic "1" $\geq$ 2.8V at 180 μa to ground.
Logic "0" $\leq$ .4V.

b. Search: Logic "1" $\geq$ 3V.
Logic "0" $\leq$ .4V.

c. Manual Fwd/Rev: Logic "1" $\geq$ 2.8V at 180 μa to ground.
Logic "0" $\leq$ .4V.

2.2 OUTPUTS

2.2.1 J3 Standard Pulse Rates

a. Rates:

1 k pps

100 pps

10 pps

1 pps

b. Duty Cycle: 80/20%

c. Positive rise on time.

d. Output Levels: Logic "0" $\leq$ .4V
Logic "1" $\geq$ 3V

e. External Load: To +5V, not less than 1K.
To ground, not less than 15K.

2.2.2 Parallel Outputs - J5

a. 42 bit BCD Time of Year

b. Output Levels: Logic "0" $\leq$ .4V.
Logic "1" $\geq$ 3V.

c. External Load: To +5V $\geq$ 1K.
To ground $\geq$ 1.5V.

2.3 ENVIRONMENT

a. Temperature: 0°C to +50°C

b. Humidity: up to 95% relative.

2.4 PHYSICAL

a. Panel Height: 1-3/4 inches.

b. Chassis Width: 17 inches.

c. Chassis Depth: 18 inches

2.2.3 Slo Code

a) Five rate serial code

b) For format see Drawing 9100-7000

c) Logic "0" $\geq$ .4V

d) Logic "1" adjustable 0V to 6V peak

e) Load 100 ohms to ground

SECTION III

OPERATING PROCEDURES

3.1 GENERAL

1. Apply 115V AC power to J6.
2. Turn on instrument by depressing the PWR switch located on the front panel.
3. Place a standard 1 kHz modulated IRIG B code on BNC connector J1 located on the rear of the unit. It does not matter if the code format has been modified to remove the 17-bit binary STOD as this portion of the time code is not used for decoding purposes in the 9200. (See 9200 specifications for modulation ratio, frequency range and amplitude requirements.)
4. After allowing approximately one minute after turn-on for the AGC to settle, the 9200 will automatically synchronize to the IRIG B time code.

3.2 ERROR BY-PASS

1. Press 0 ERROR. The 9200 will now respond to each time frame of the IRIG B code. Any degradation of the input code may cause an erroneous reading on the 9200 Time Code Reader.
2. Press 3 ERROR. The 9200 will now sync to the IRIG B input code, then automatically lock out its own sync circuits and just monitor the input code for time differences. Frame errors are counted; however, the 9200 synchronization is not disturbed unless three consecutive errors are counted. If frame errors are separated by valid frame, the error counter is reset to zero; therefore, resynchronization can only take place on the fourth frame after counting three consecutive errored frames. This mode can be extremely useful when input time code is noisy or being derived from a poor or spliced tape.

3. BY-PASS. Note: Prior to pressing this mode selector switch, the 9200 must be synchronized in either the 0 ERROR or 3 ERROR mode, then after synchronization transferred to the BY-PASS mode by pressing its selector. Once in this mode, all synchronizing functions are locked out and the 9200 will act as an elapsed time generator updating on the 1 kHz IRIG B carrier. This mode can be useful on an extremely poor input time code. (Note: one of the sync mode switches must always be depressed for normal operation.)

3.3 FWD/REV MODES

The 9200 is provided with automatic direction sensing, therefore, it is not necessary to manually select forward or reverse operation. If manual operation should be desired, this can be accomplished by removing the jumper between E10 and E12 on card assembly 15033 and placing a jumper between E11 and E12 on the same card. When operating with manual orward/reverse control, a logic "1" on pin 45 of J5 will select forward translation mode and conversely a logic "0" will select the reverse mode.

3.4 EXTERNAL CLOCK INHIBIT

A logic "1" applied to pin 43 of J5 will inhibit clock updating of the Reader. This is primarily used to freeze the display in tape search systems when the tape transport is stopped. A logic "0" will allow count to resume.

3.5 INTERNAL FILTER CONTROL

An internal 3 KC low pass filter has been provided in the 9200 TCR for use in the playback (x1 speed ratio) mode only. To activate the filter, a logic "0" must be applied to pin 44 of J5. A logic "1" (or an open circuit) will remove the filter for high speed translation.

3.6 TURN OFF PROCEDURE

Press the PWR switch a second time.

SECTION IV
ADJUSTMENTS

4.1 Assembly 15005 ACG Amplifier

a. Pot R38 code stripper adjustment. Set for one phase "C" pulse for every carrier cycle of the mark amplitude pulse.

b. Pot R15: Set for DC balance on pin 6 and pin 8 of AGC Amplifier A1.

4.2 Assembly 940003 Power Supply

R21 adjust output level of the +5V regulator. Should be set to +5V ±2%.

4.3 Assembly 15068 Slow Codes

R19 level adjustment range .5V to +6V with 100 ohm load.

SECTION V

THEORY OF OPERATION

The Model 9200 is a device which requires a serial coded input and "reads" or "decodes" or "translates" this input to some other form, usually parallel time data.

In order to better understand the logic organization of the 9200, let's first review the basic configuration of a typical reader.

Figure 1 shows a simplified diagram of a typical time code reader. The significant points to a time reader are:

1. Input Amplifier. Usually this is an AGC type amplifier. Its function is to provide a constant amplitude signal to the decode and detection circuitry.

2. Serial-to-Parallel Converter. This is the heart of the unit. The function here is to detect digital data in the input format and assign it to storage in the time accumulator. This portion contains the necessary circuits to synchronize the frequency dividers.

3. Frequency Dividers. These counters divide the code carrier frequency. Once synchronized by the decoding circuitry in the serial-to-parallel section, this counter provides the terms necessary to index the digital data contained in the input code thus allowing the locating of each code bit and proper assignment to accumulator storage. Another important factor is to provide a 1 pps signal to update the time accumulator.

4. Time Accumulator. This section is a counter whose function is to store the value being read from the input code. It is updated

with the 1 pps signal above and is permuted to count in the format of the time code; usually seconds, minutes, and hours. Day of year may sometimes be provided if required and if it is contained in the input time code. The accumulator is the basis for most outputs required by the unit.

5. Display. This section takes the time accumulator data displays it for interface to the user.

The 9200 is shown functionally in Figure II. Each logic section shown by dotted lines relates also to the mechanical configuration of the unit. Each section is contained on one circuit board in the unit.

Mechanically and logically there are two main logic sections in the unit. These are:

1. Decoder Section

2. Basic Section

The decoder contains all of the decoding and synchronization circuits required. The basic contains the major and minor time counters. The remaining circuit assemblies are very functional and for the most part perform single operations.

1. AGC. The automatic gain control amplifier assembly contains the input amplifier and the Schmitt triggers required to normalize the input and derive the necessary clock signals for the decoder.

TYPICAL TIME CODE READER

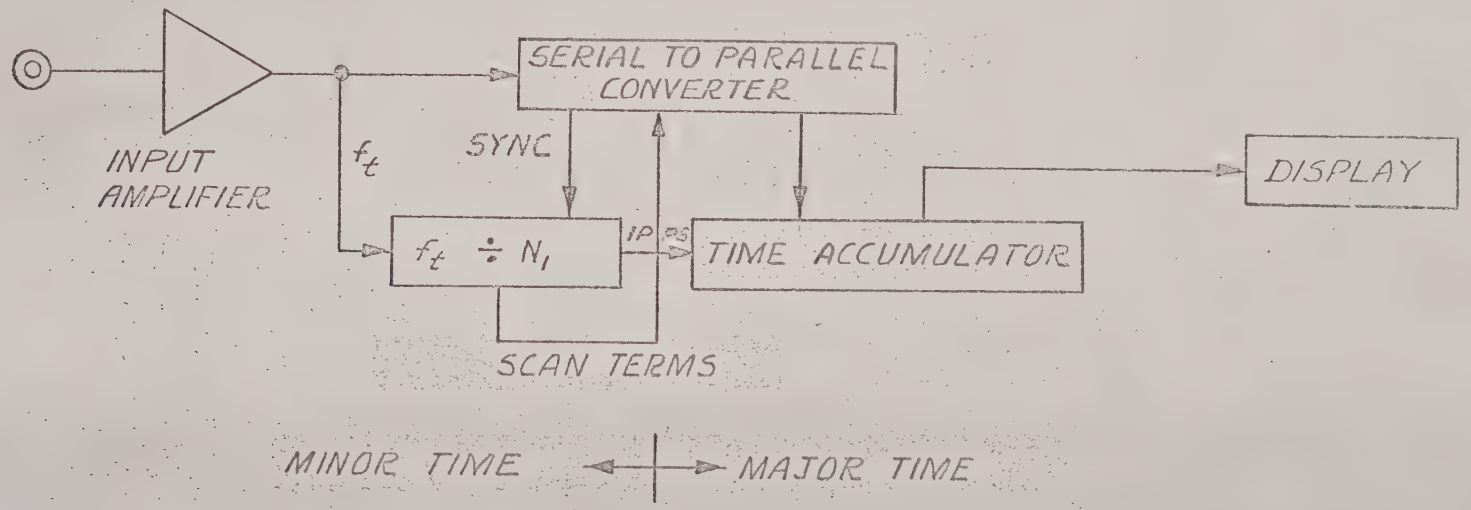


FIGURE 1

The AGC amplifier is wideband so as to make the unit operational where variations of input signal frequency as well as amplitude are experienced such as in tape search applications.

Generally if a reader is used as a single purpose unit such as to only read code at a single rate and display it, the AGC circuits can be narrow-band. To make the unit more adaptable to different types of applications, we have provided a 100 MV to 10 volt dynamic range and a frequency response of 25 Hz to 300 kHz. The circuit does not require adjustment over this range.

After the input signal is normalized by the AGC, preset level Schmitt triggers develop clock signals used for decoding. The most important is "ZA" which occurs at the positive zero axis crossing of the carrier. This signal is used throughout the unit for clocking and synchronization. "ZC" is the mark clock which occurs only each half cycle of the carrier modulation (mark amplitude cycles). Figure II shows a typical modulated signal. Two cycles are modulated. Examples of ZA and ZC are shown relative to the signal. Observe also the other definitions provided. The AGC is an extremely important portion of the unit, and actually represents the interface between analog and digital domains.

2. Decoder. The output clocks from the AGC are connected to the decoder assembly; here the entire translation process takes place. The functions performed by the decoder assembly are:

   a. Reconstruct dc envelope of the time code

b. Determine code pulse rate

c. Determine time frame sync (frame reference mark)

d. Synchronize minor time

e. Code bit storage and accumulator loading

f. Synchronization mode error detection and storage

g Automatic forward-reverse sensing (optional)

Implementations of the decoder, which are of benefit to the user, are described below.

a. DC Envelope Reformation. The amplitude modulation of the time code signal represents a pulse width modulated dc envelope. The key to reliable translation or reading is the reconstruction of this envelope. Once this has been done, it is a simple process to examine the dc signal for the presence of binary information. The clocks from the input shapers and three flip-flop storage counters are used in this operation. The significant point is that a cycle can be dropped or a noise spike can occur to add a pulse and the reconstruction of the envelope will not be affected. Thus, we say that the unit has "single cycle dropout protection."

b. Determine Code Pulse Rate: This is as simple as it appears. The first step to synchronization of the input is to detect the pulse rate of the input code. This is done by examining the dc envelope reconstructed in step (a) and developing a clock at the leading edge of this signal. In format IRIG B this clock would be 100 pps since the pulse rate of the coded information is 100 pps (see Figure III). This term is called "mark sync" (MS). For IRIG B, the dc envelope obtained from the three counters in step (a) will be exactly 2 milliseconds late with respect to the "on time"

point (modulation point) of the serial code. This is due to the logic implementation in the decoder discussed above.

With MS occurring at 100 pps less 2 milliseconds, we know that the counter dividing 1 kHz must read "2" at its leading edge. Thus to synchronize the milliseconds counter all that is needed is to set it to a "2" with the MS clock. With the milliseconds counter synchronized, we now have a means to measure pulse widths of the input code from zero to 9 milliseconds.

c. Determine Frame Sync.

d. Synchronize Minor Time.

Let us summarize what we now know and have accomplished.

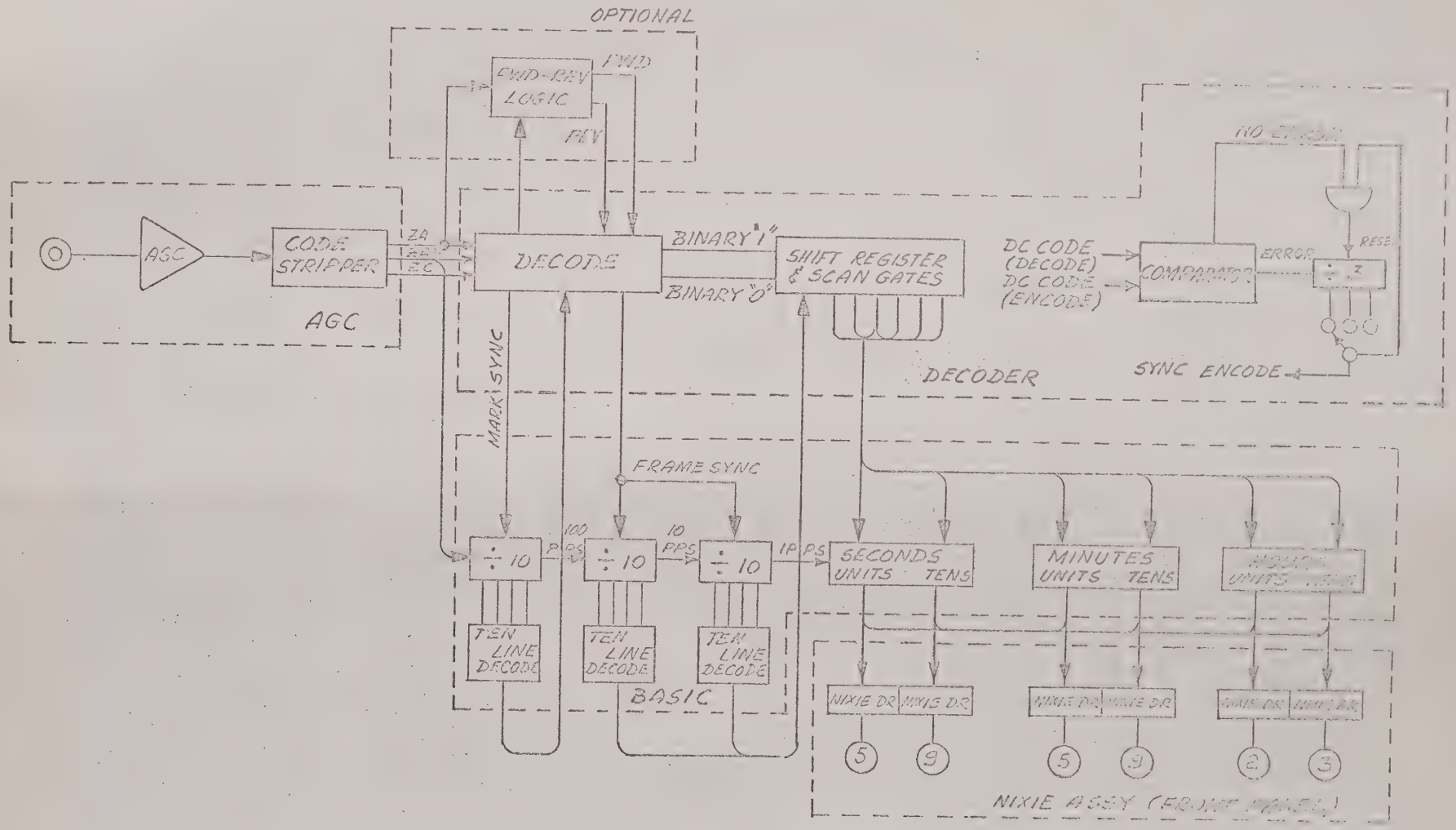
(1) We have a dc pulse train of the code.

(2) We have a counter dividing 1 kHz in synchronization with the dc code envelope. Thus, each code bit period is divided into 10 equal parts.

(3) The IRIG B reference mark is two consecutive 8 millisecond bit periods.

(4) IRIG B reference occurs at a 1 pps rate.

If we take the dc code and examine it at a count of 8 in the milliseconds counter, we will detect each 8-millisecond-wide pulse. When two consecutive pulses occur, we know we have received a 1 second reference. We also know that the counters counting 100 pps and 10 pps must be zero at this time. We set them to zero, therefore, at the leading edge of "F.S." (Frame Sync).



BLOCK DIAGRAM MODEL 9200
TIME CODE READER

e. Code Bit Storage and Accumulator Loading. Now that we have a counter dividing 1 kHz (IRIG B code carrier) and synchronized to the incoming code, we can locote any point within the format to a resolution of 1 millisecond. Furthermore, we can also "measure" the pulse width and therefore determine "1's" and "0's", which are noted to be of 5 and 2 millisecond duration, respectively.

A binary "1" is determined by examining the reconstructed dc envelope at a millisecond count of 5. A 4-bit shift register is successively loaded with the detected binary "1's" as they occur in the serial format. The result is therefore a continuous stream of "1's" and "0's" flowing through the 4-bit register.

Since the minor time counter (milliseconds, .01 seconds, .1 seconds) is synchronized with the input code, any 1 millisecond interval can be pin-pointed within the serial train. Actually, it is only necessary to locate an interval of 40 to 50 milliseconds -- in other words, an interval which contains 4 bits of the code. Therefore, six "load" periods are defined by gates "looking" at the minor time counter. Each of the load gates connects a 4-bit decade in the time accumulator to the shift register. As the data of interest is shifted in, it is loaded into the decade associated with the 4 bits. In this manner units of seconds, tens of seconds, units of minutes, etc., are loaded seauentially from the shift register to the accumulator as the code is read.

The 36 bits of seconds, minutes, and hours and days are read and loaded in the first 400 milliseconds of the format. However, this time word represents a 1 second interval which began 400 milliseconds before (at the "on time" reference

point). The output time must be placed "on time". That is, it is required that the output time update at the 1 second reference, which occurred 400 milliseconds before the entire time word is read. If, however, we take advantage of the fact that the synchronized minor time counter will supply a 1 pps signal exactly at the reference mark, we can then add this to the value in the accumulator. This, in effect, is anticipating the next time word value, and puts the output exactly "on time".

To summarize, the decoding process takes at least two time frame periods to synchronize to the code input. First, the code pulse rate synchronizes the least significant bit counter (milliseconds). Next, "frame sync" is determined by using this milliseconds data and the dc level envelope of the input code. This data allows complete synchronization of the minor time counter. Once this is done, "1's" and "0's" of the code can be loacted and placed in appropriate storage in the time accumulator. The accumulator is then updated with 1 pps to place it "on time". The entire process is repeated for each frame but does not actually cause any change in the output as long as the reader remains synchronized because the accumulator is being updated "on time" by the 1 pps pulse prior to the decoded time availability (400 milliseconds after "on time").

f. Synchronization Mode Error Detection and Storage. Another function contained on the decode assembly is the synchronization mode logic. In order to explain this function, it is necessary to assume that the unit is developing a serial code (before we have covered the serial code encoder section).

The "synchronization mode" function is designed to provide protection to the outputs in the event decoding errors occur. These errors can be due to many things such as noise, dropouts, voltage transients, etc. For example, if a noise burst or voltage transient occurred which caused a code error, thus wiping out a 1 second frame, the output would continue to read the correct code as long as carrier sync was maintained.

Obviously, if the carrier were gone completely for a time frame, the unit could not maintain sync. The synchronization mode feature increases the noise immunity of the unit significantly and is an added aid to tape search requirements.

The synchronization mode circuitry compares the reconstructed dc level with the generated code pulse train from the encoder. Thus, time contained in the time accumulator is compared bit-by-bit with the input code. If an error is detected, it is recorded and stored in the 3-bit counter. The next frame is examined. If another error is detected, it also is stored by adding it to the first, and so forth. Note that only one error per frame is considered.

The 9200 provides front panel switches to select the error frame bypass mode. Three conditions are provided by the unit. These are:

(1) Zero Frames

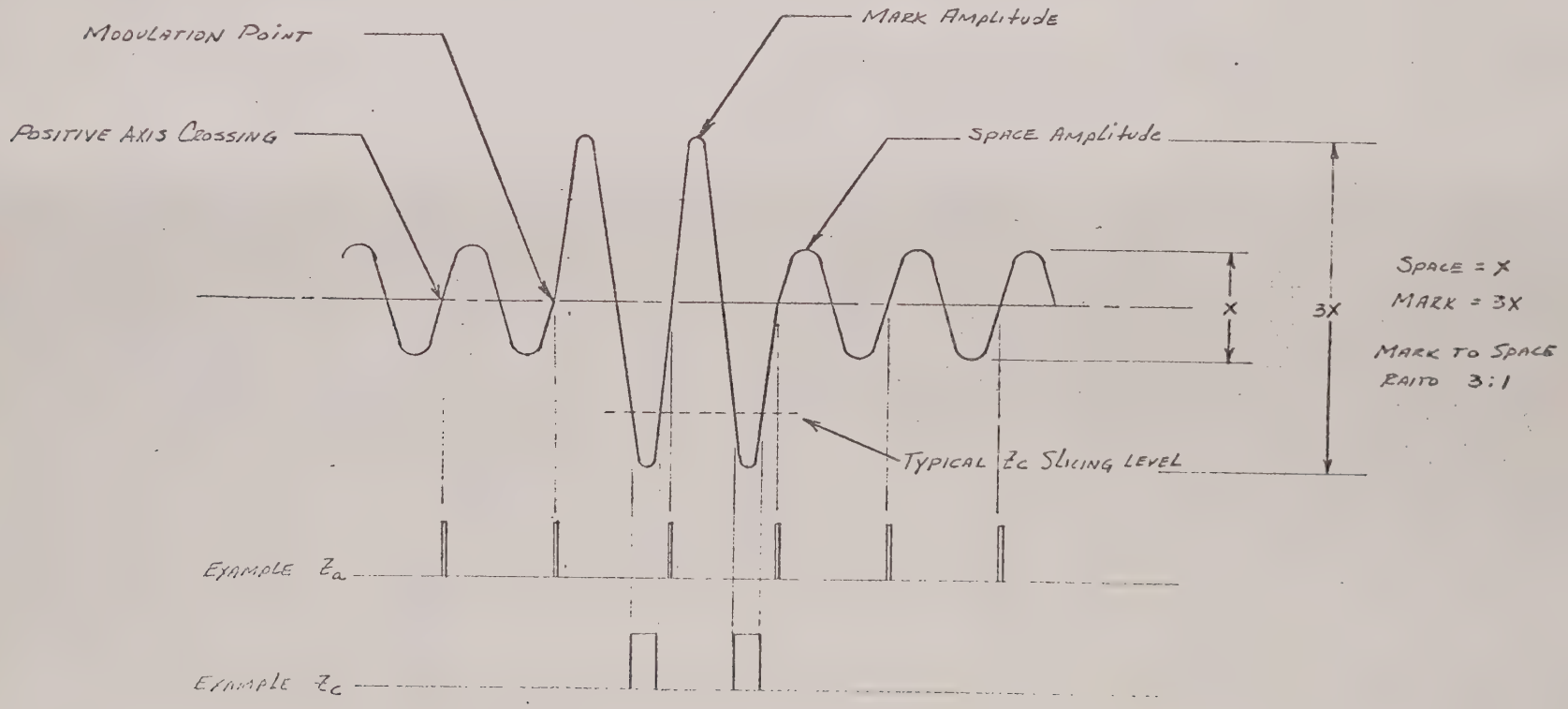
(2) Three Frames

(3) oo(all) Frames

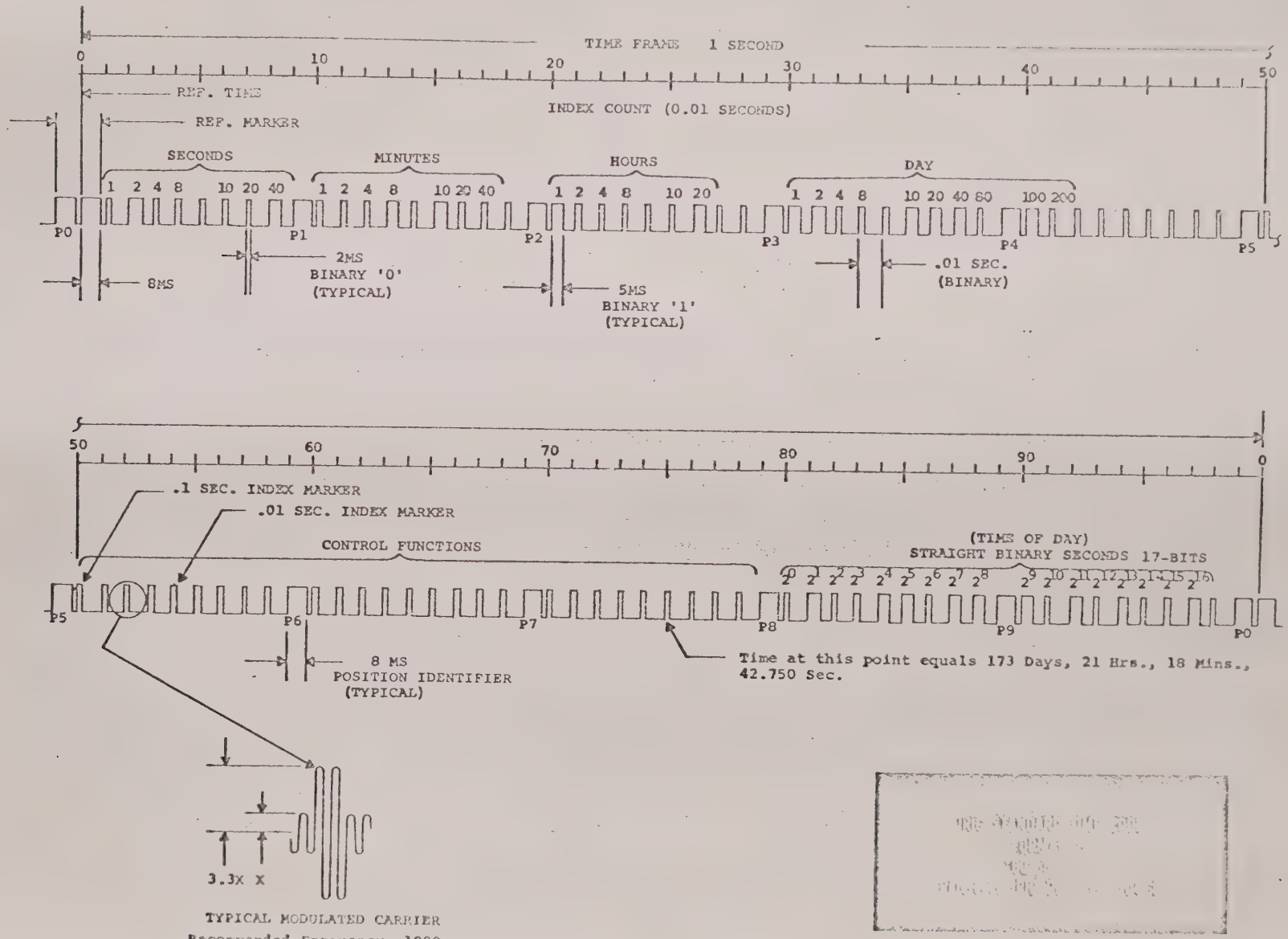
With "Zero Frames" selected, the unit is a slave reader and synchronizes to each frame.

With "Three Frames" selected, the unit will accumulate three error frames without resynchronizing. If three consecutive errors are recorded, the next frame (fourth) is used to resynchronize the unit. The error counter is reset if no error is detected on the next frame (fifth). If, however, an error condition continues, synchronization again is accomplished immediately. This is continued until two consecutive frames agree. Once synchronized, the unit "free runs," so to speak, with synchronization disallowed until at least three consecutive frame errors are detected.

When "oo" is selected, the synchronization of the unit is continuously inhibited and the unit acts as a generator using the carrier input as a clock.

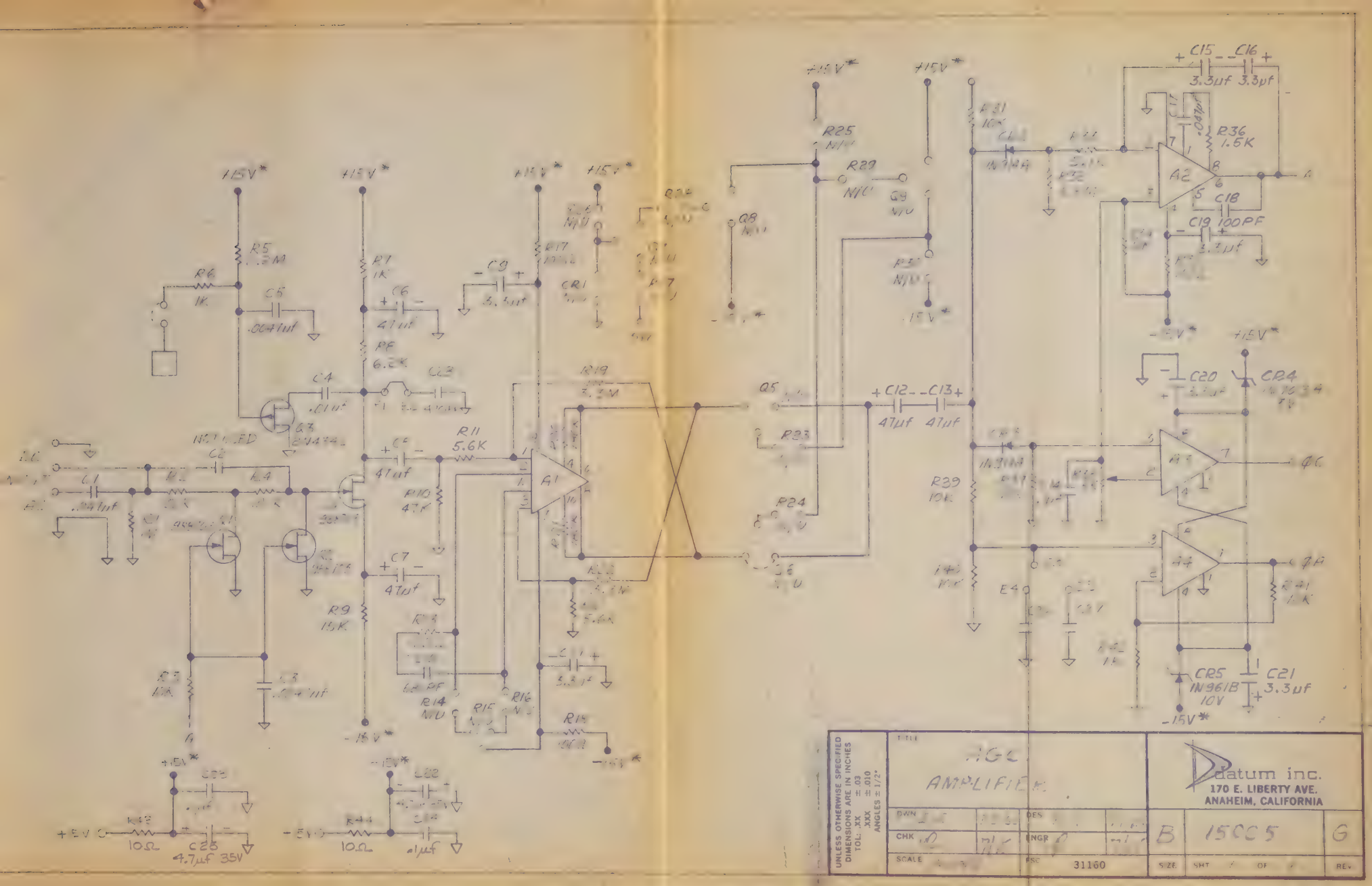


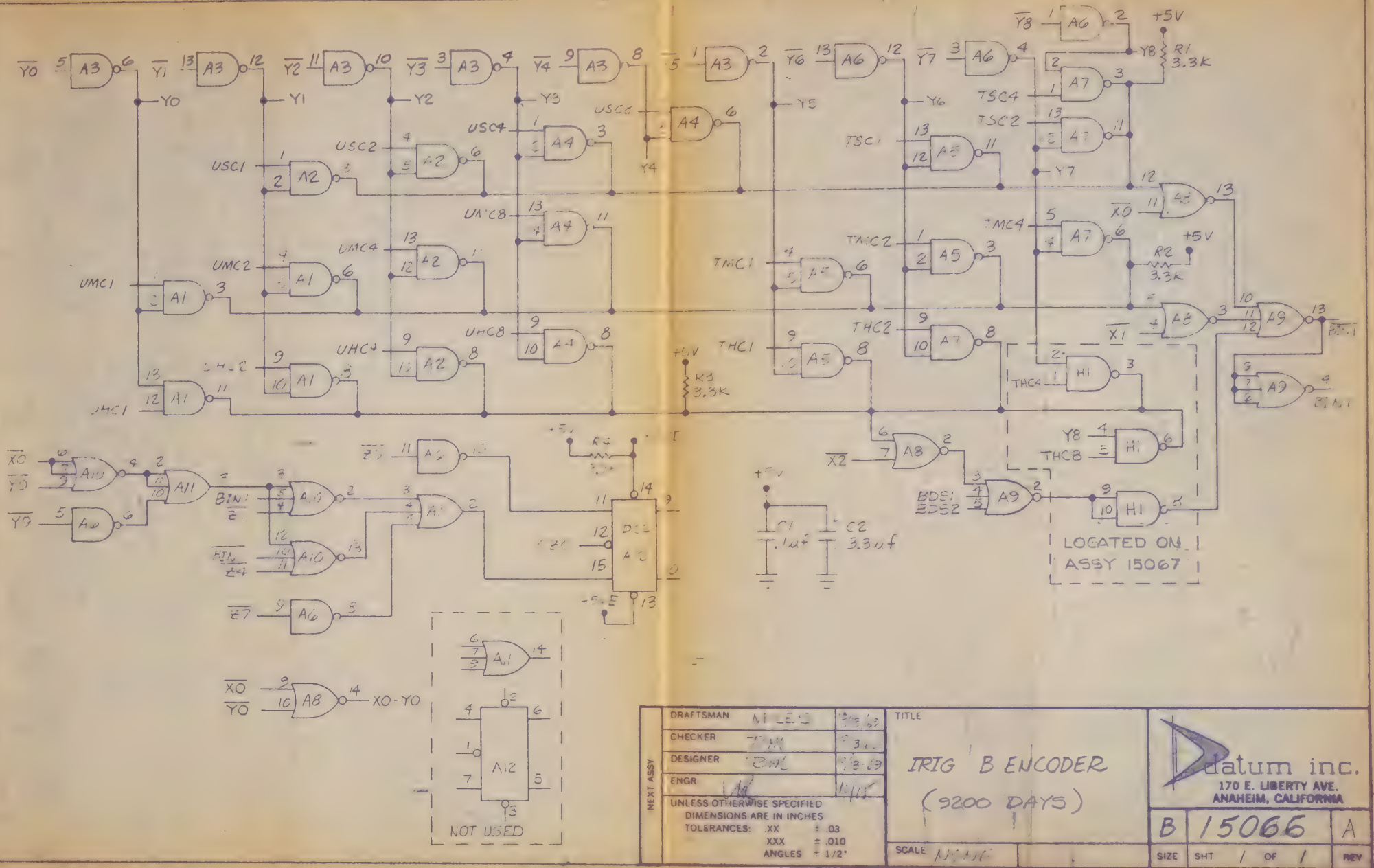
Typical Modulated


TIME FRAME 1 SECOND
0
10
20
30
40
50
REF. TIME
INDEX COUNT (0.01 SECONDS)
REF. MARKER
SECONDS
MINUTES
HOURS
DAY
1 2 4 8 10 20 40
1 2 4 8 10 20 40
1 2 4 8 10 20
1 2 4 8 10 20 40 80 100 200
P0
P1
P2
P3
P4
P5
8MS
2MS
BINARY '0'
(TYPICAL)
5MS
BINARY '1'
(TYPICAL)
.01 SEC.
(BINARY)
50
60
70
80
90
0
.1 SEC. INDEX MARKER
.01 SEC. INDEX MARKER
CONTROL FUNCTIONS
(TIME OF DAY)
STRAIGHT BINARY SECONDS 17-BITS
P5
P6
P7
P8
P9
P0
8 MS
POSITION IDENTIFIER
(TYPICAL)
Time at this point equals 173 Days, 21 Hrs., 18 Mins., 42.750 Sec.
3.3X X
TYPICAL MODULATED CARRIER
Recommended Frequency, 1000 cps

SECTION VI
LIST OF DRAWINGS

1.	AGC	15005
2.	IRIG B Encoder	15066
3.	Decoder	15033
4.	Basic	15064
5.	Display Logic	15024
6.	Slo Codes	15068
7.	Parallel Outputs	15067
8.	Days Scan	15065
9.	Power Supply	940003
10.	Top Assembly Drawing	9200-602
11.	5-Rate Slow Code	9100-7000


+15V*
-15V*
R5 1.2M
R6 1K
C5 .0047uf
R7 1K
C6 47uf
PF 6.2K
C4 .01uf
C12 47uf
C13 47uf
R11 5.6K
R10 47K
C7 47uf
R9 15K
R8 1K
C3 .047uf
R14 N/U
R15 N/U
R16
R19
C1 .047uf
C2
R1
R4
R2
R3
A1
A2
A3
A4
Q5
Q6
Q7
Q8
Q9
R23
R24
R25 N/U
R29 N/U
R31 10K
R32
R36 1.5K
C18
C19 100PF
3.3uf
C15 3.3uf
C16 3.3uf
C20
CR4 IN746A 3.3V
R39 10K
R41 1K
CR5 IN961B 10V
C21 3.3uf
R42 10Ω
C25 4.7uf 35V
R44 10Ω
C24 .1uf
AGC AMPLIFIER
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°
DWN
CHK
ENGR
DES
SCALE
FSC 31160
SIZE B
15005
SHT OF
REV G



NEXT ASSY	DRAFTSMAN	
	CHECKER	
	DESIGNER	
	ENGR	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE

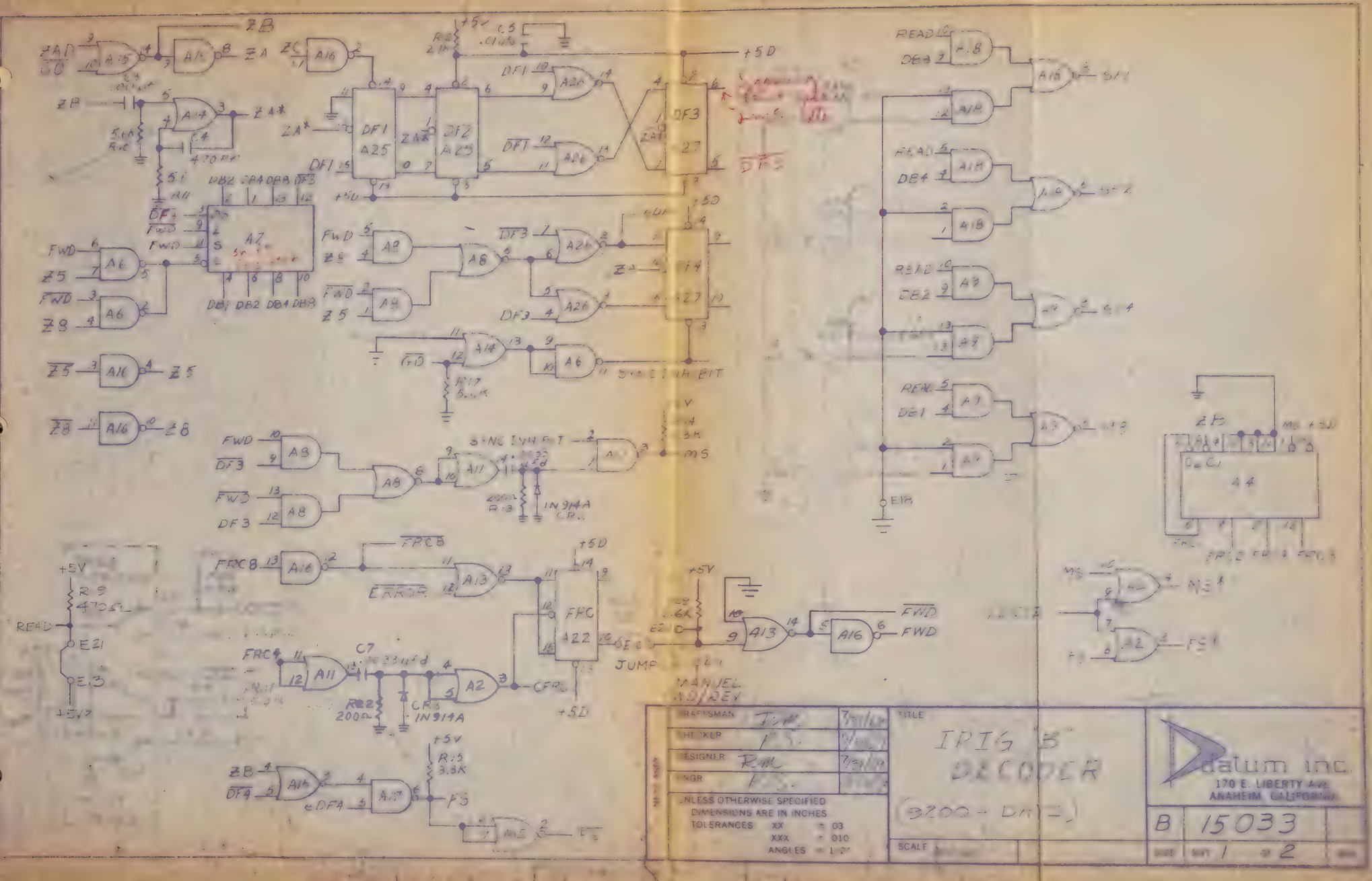
IRIG B ENCODER

(9200 BAUD)

SCALE

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B	15066	A
SIZE	SHT 1 OF 1	REV


ZB
ZA
ZC
+5V
+5D
DF1
DF2
DF3
DF4
DF5
ZA*
ZB*
FWD
READ
DB2
DB4
DB8
DB1
SYNC LYH BIT
GND
MS
FRCB
ERROR
FRC
JUMP
CFR
R9 470Ω
R13 3.3K
R17 5.1K
R2 2.1K
C5 .01 mfd
C7 .023 mfd
C4 470 PF
R22 200Ω
CR3 IN914A
E21
E13
E18
E19
E20
E22
E23
E24
E25
E26
E27
E28
E29
E30
E31
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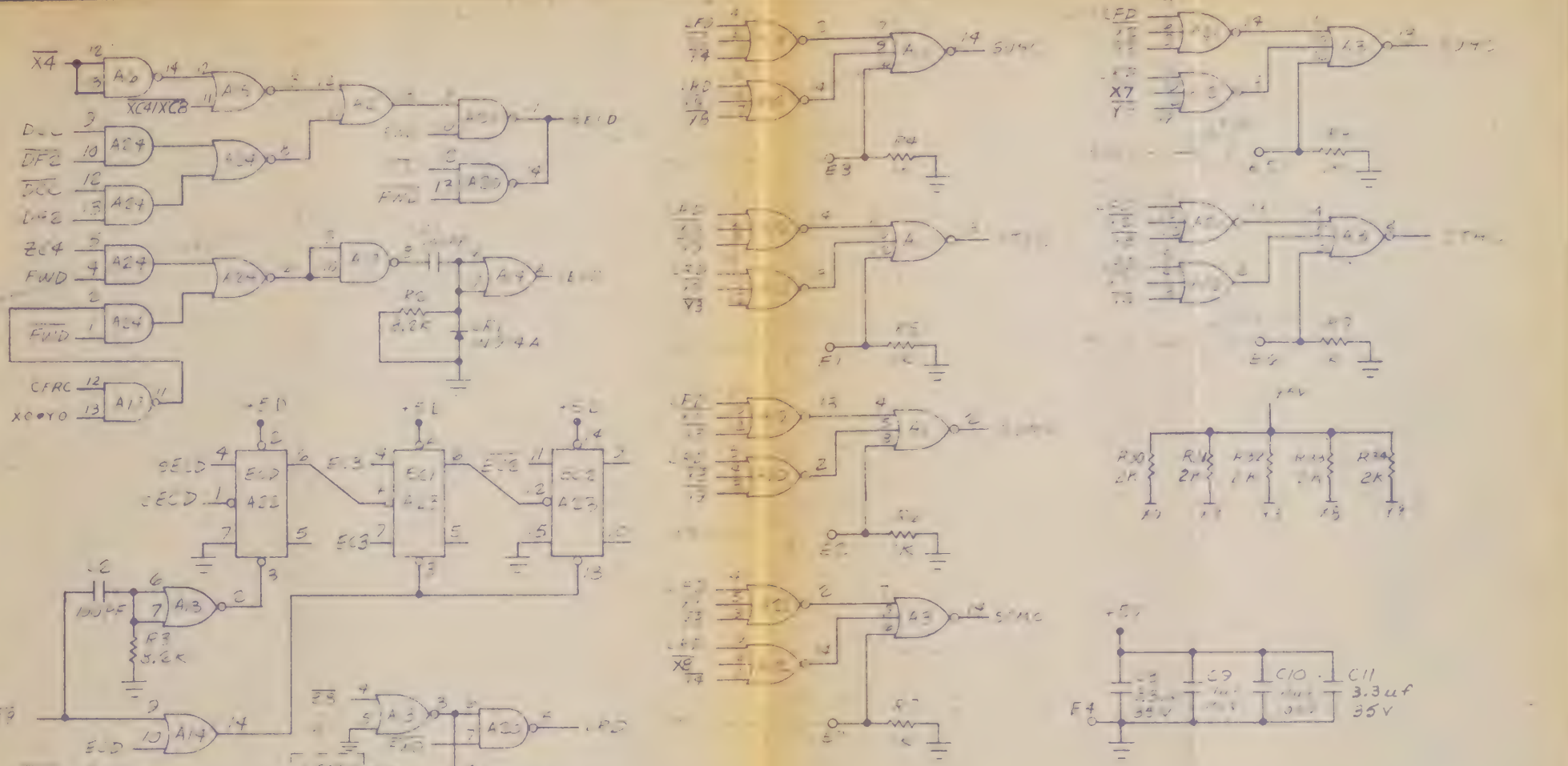
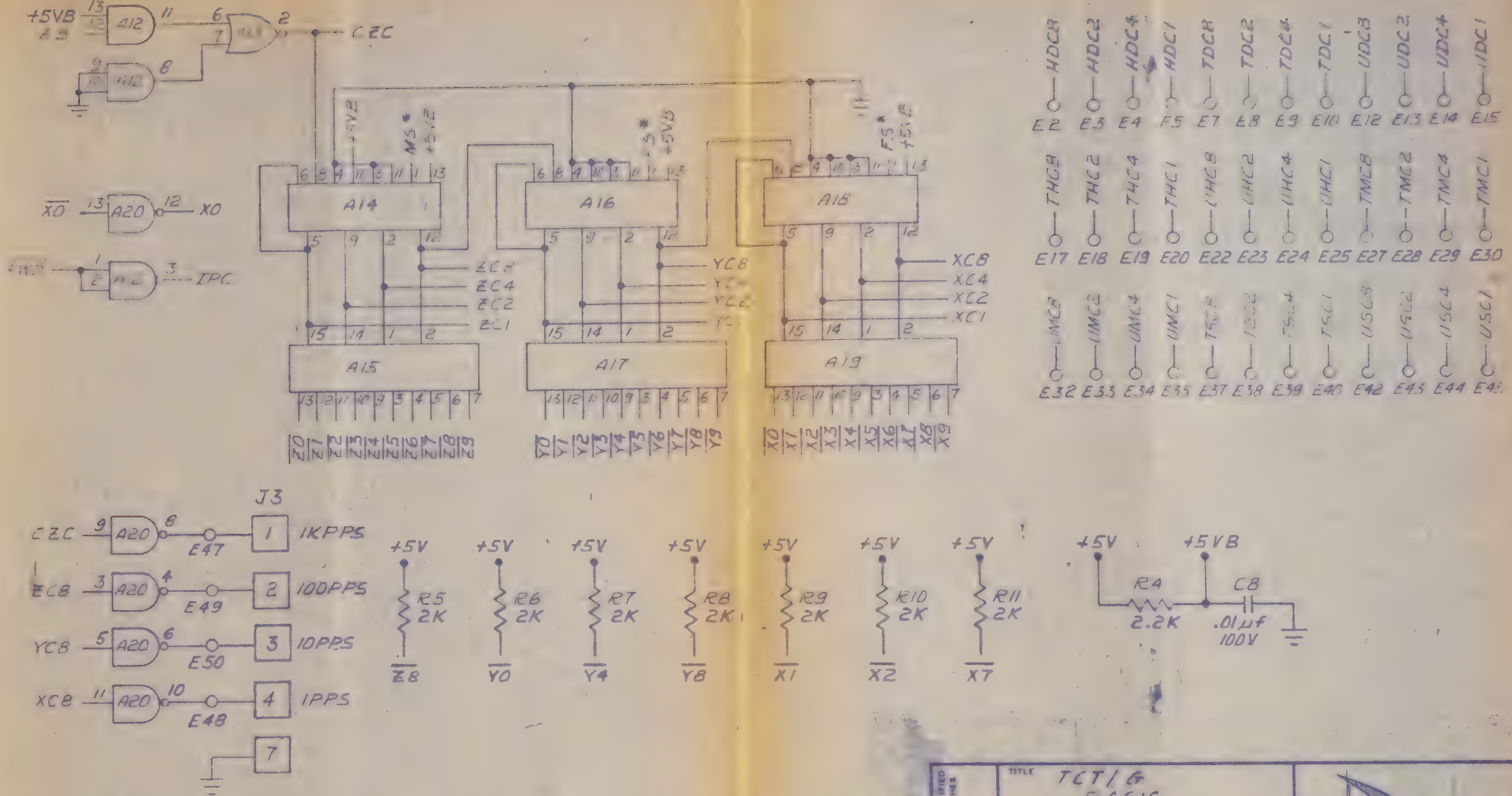

X4
XC4 XC8
DFC
DFC
FWD
FWD
CFRC
XC YC
SEC D
FWD
PC
8.2K
+5V
PE
1.5K
S2
S3
S4
ERROR
IRIG B
DECODER
(2100-1415)
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
DRAFTSMAN
CHECKER
DESIGNER
ENGR
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES .XX ± 03
.XXX ± 010
ANGLES ± 1/2°
NEXT ASSY
SCALE
SIZE
15033
SHT 2 OF 2
REV



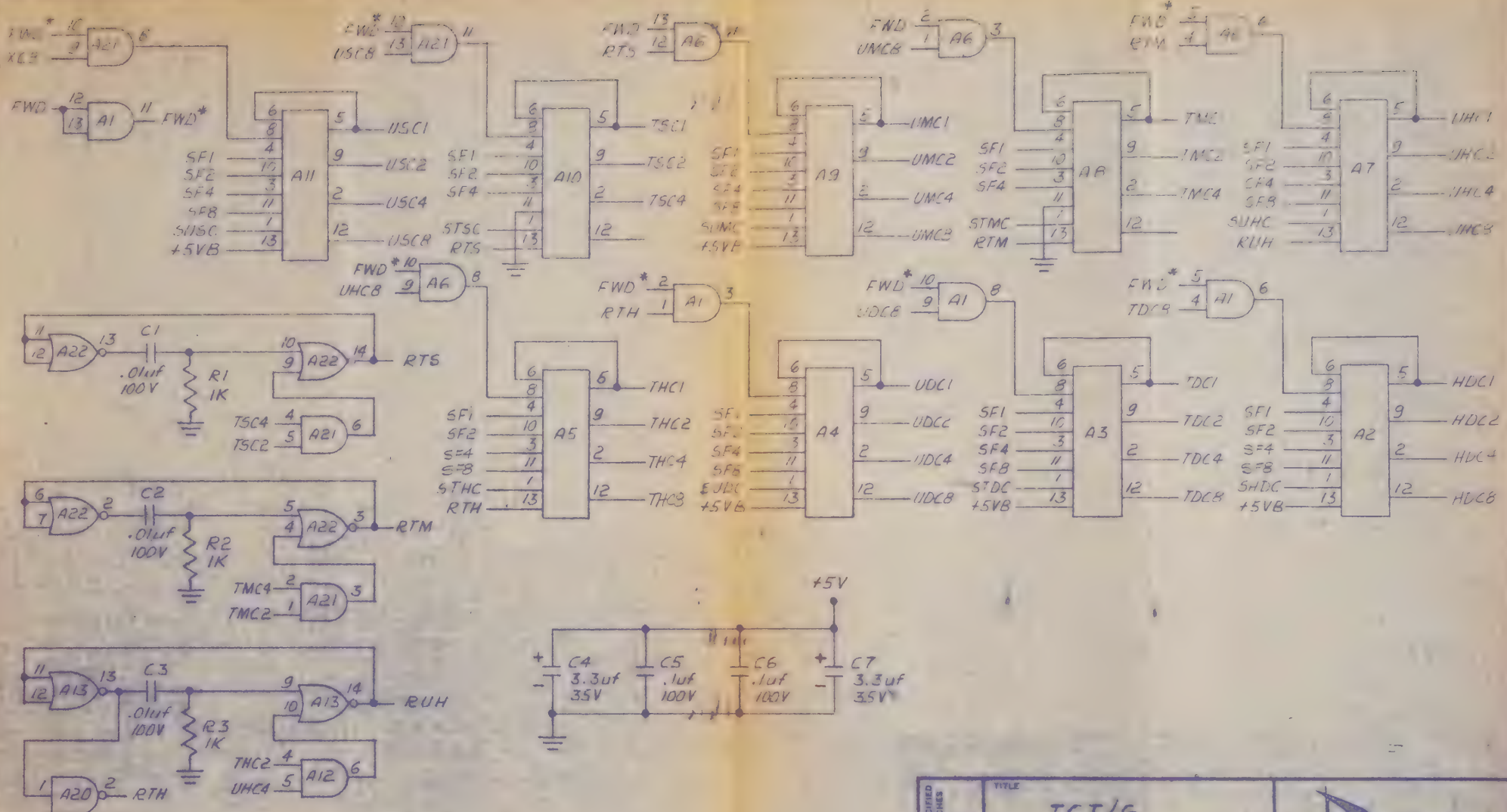
FWD & REV

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL XX ± .03 XXX ± .010 ANGLES ± 1/2°

TITLE TCT/G BASIC 920Q DAYS

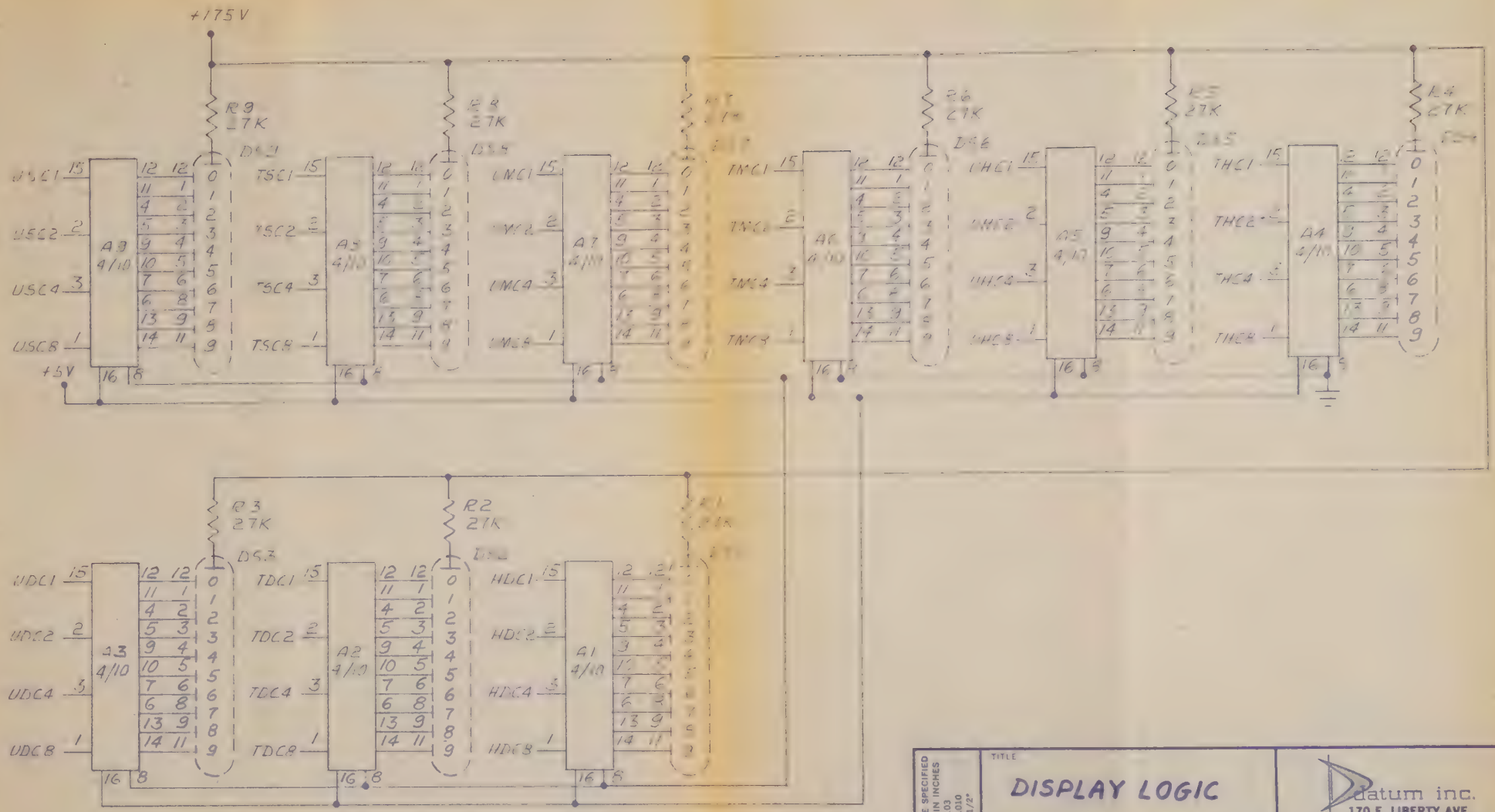
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	10/1/69	DES	DM	7/2/69	B 15064
CHK	DM 7/2/69	ENGR			
SCALE NONE		FSC 31160			SIZE SHT 1 OF 2 REV



FWD & REV

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°	TITLE: TCT/G BASIC 9200 DAYS			datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA	
	DWN RM 10/16/69	DES RM 7/2/69		B	15064
	CHK RM 7/3/69	ENGR			
	SCALE	FSC 31160		SIZE	SHT 2 OF 2 REV



1. ALL RESISTORS ARE ¼W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED

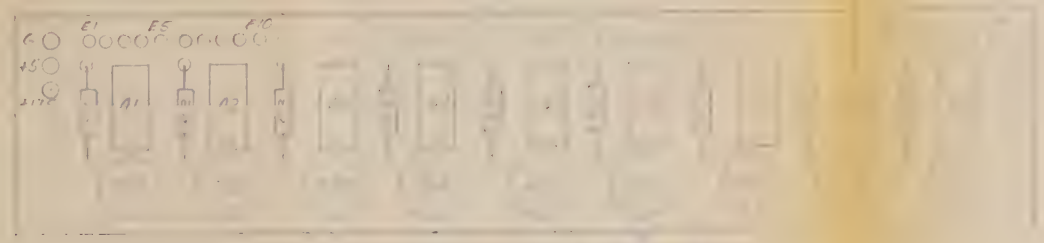
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE: DISPLAY LOGIC

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN IC	6-30	DES RM	7/2/69	B	15024
CHK RM	7/2/69	ENGR			
SCALE NONE		FSC 31160		SIZE	SHT 1 OF 2 REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



BOTTOM VIEW
SCALE 4/1

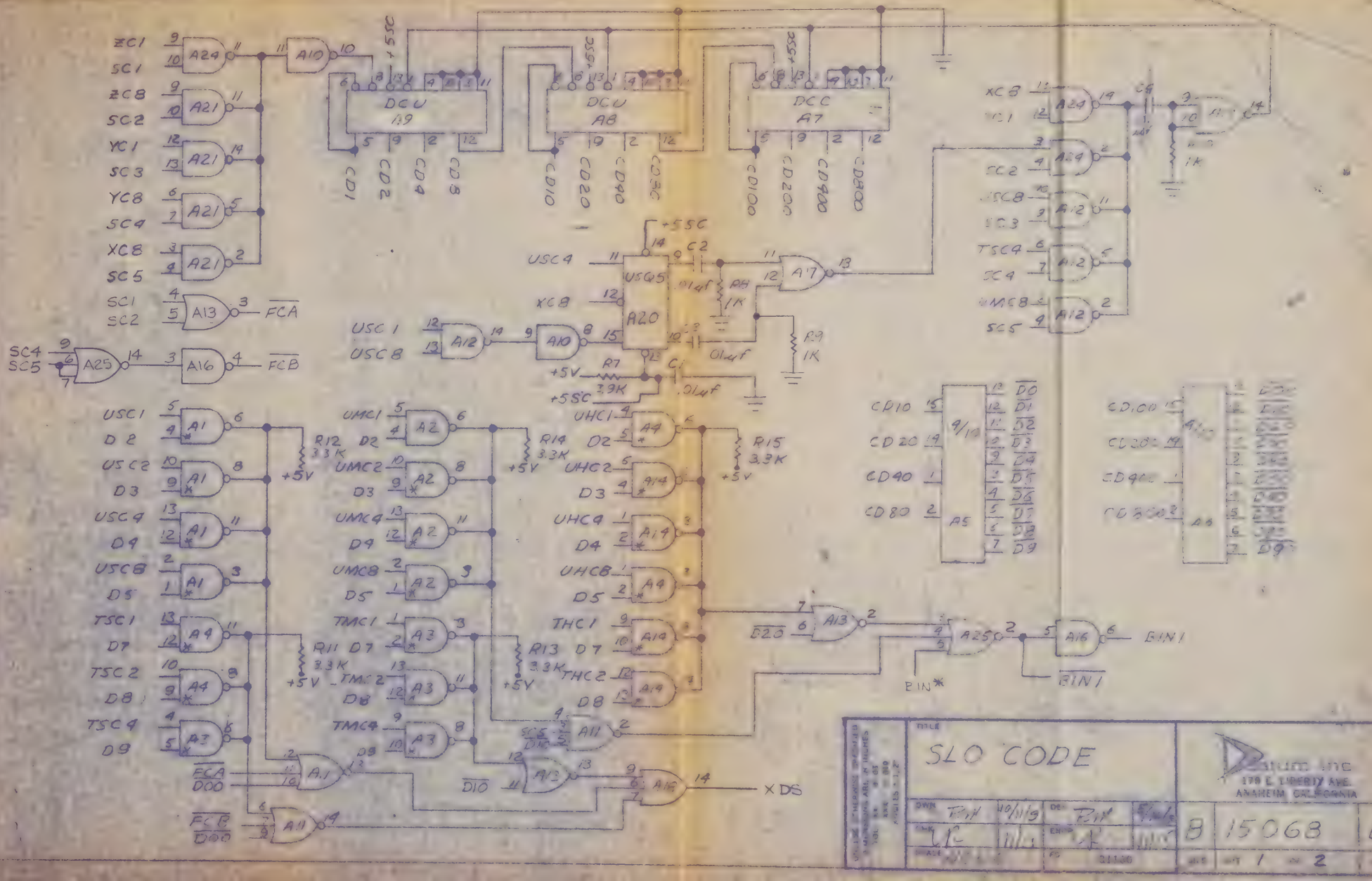
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOL: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

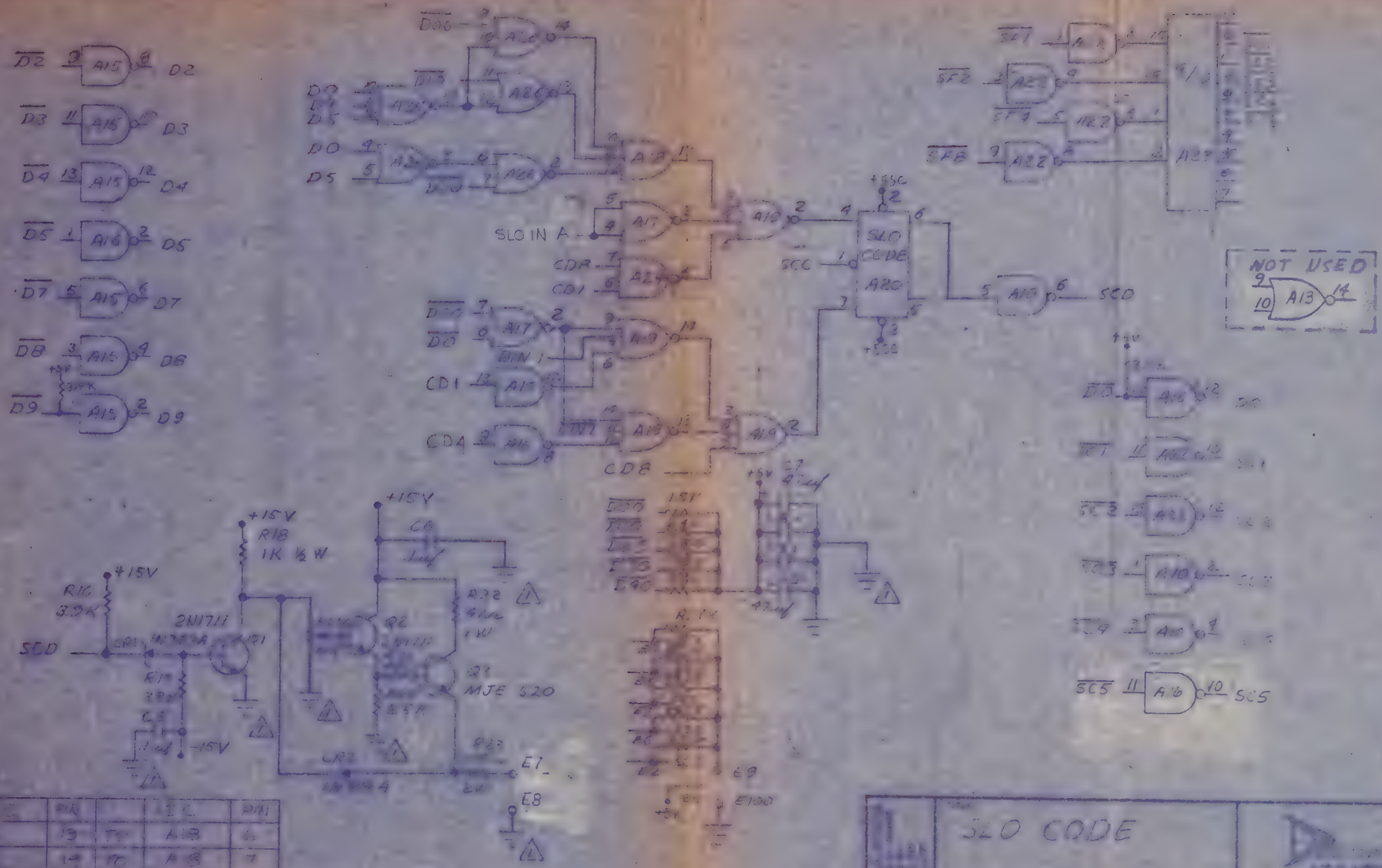
TITLE

DWN		DES		
CHK		ENGR		
SCALE		FSC 31160	SIZE	SHT OF REV

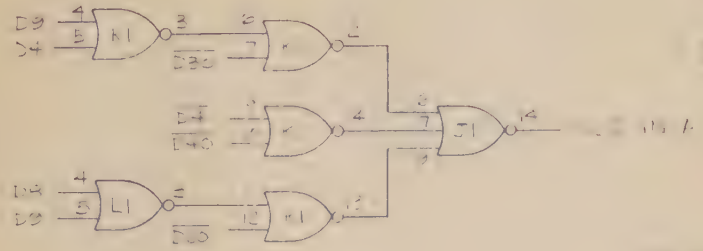
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

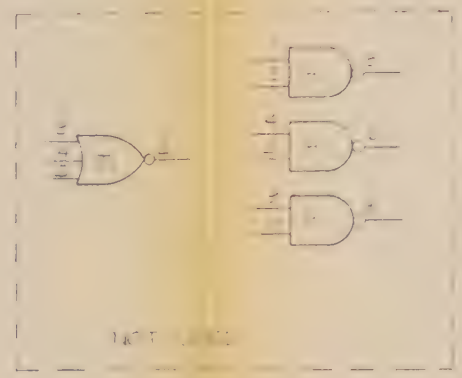
DIETZGEN 1 FORM 30


ZC1
SC1
ZC8
SC2
YC1
SC3
YC8
SC4
XC8
SC5
SC1
SC2
SC4
SC5
USC1
D2
USC2
D3
USC4
D4
USC8
D5
TSC1
D7
TSC2
D8
TSC4
D9
UMC1
UMC2
UMC4
UMC8
TMC1
TMC2
TMC4
UHC1
UHC2
UHC4
UHC8
THC1
THC2
DCU A9
DCU A8
DCC A7
CD1
CD2
CD4
CD8
CD10
CD20
CD40
CD80
CD100
CD200
CD400
CD800
+5SC
USC5 A20
XC8
USC1
USC8
+5V
R7 3.9K
R9 1K
R12 3.3K
R14 3.3K
R15 3.3K
R11 D7
R13 D7
D2
D3
D4
D5
D7
D8
D9
FCA
FCB
D00
D10
D20
D40
D80
XDS
BIN*
BIN!
A5
A6
TITLE
SLO CODE
DWN
CHK
APVD
DES
ENGR
PM
8
15068
B
SCALE
SHT 1 OF 2

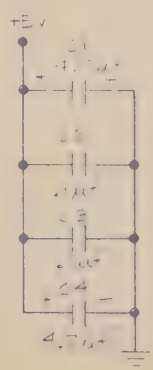

SLO IN A
SLO CODE
A20
SCC
SCD
NOT USED
A13
+15V
-15V
2N7111
MJE 520
R18
1K ½ W
SLO CODE
B 15068 E

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	CORRECTED LO[illegible] SYMBOL	3 JAN 74	





BE	(SEARCH)	F • FILTER
BF	(M-FWD/REV)	E - E11
BH	($\overline{GO}$)	E15-10
BJ	(GND)	E1-1
BK	(GND)	E2-1
BL	(GND)	E3-1
BM	(GND)	HA1-1
BN	(GND)	HA2-1
BP	(GND)	HN2-1

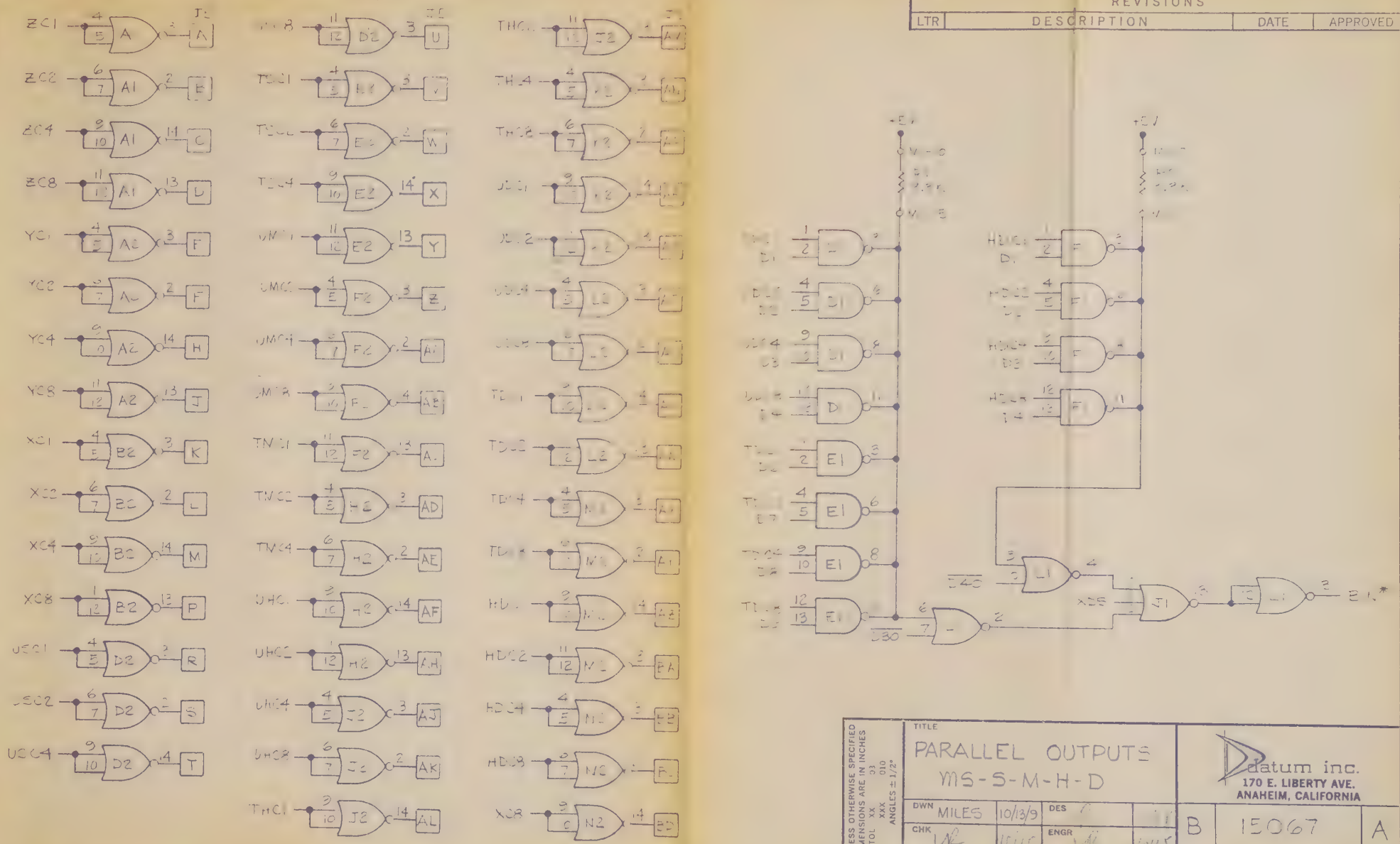


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL XX ±.03 XXX ±.010 ANGLES ±1/2

TITLE
PARALLEL OUTPUTS
ms-S-M-H-D

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN		DES		B	15067	A
CHK		ENGR				
SCALE NONE		FSC 31160		SIZE	SHT 1 OF 2	REV



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

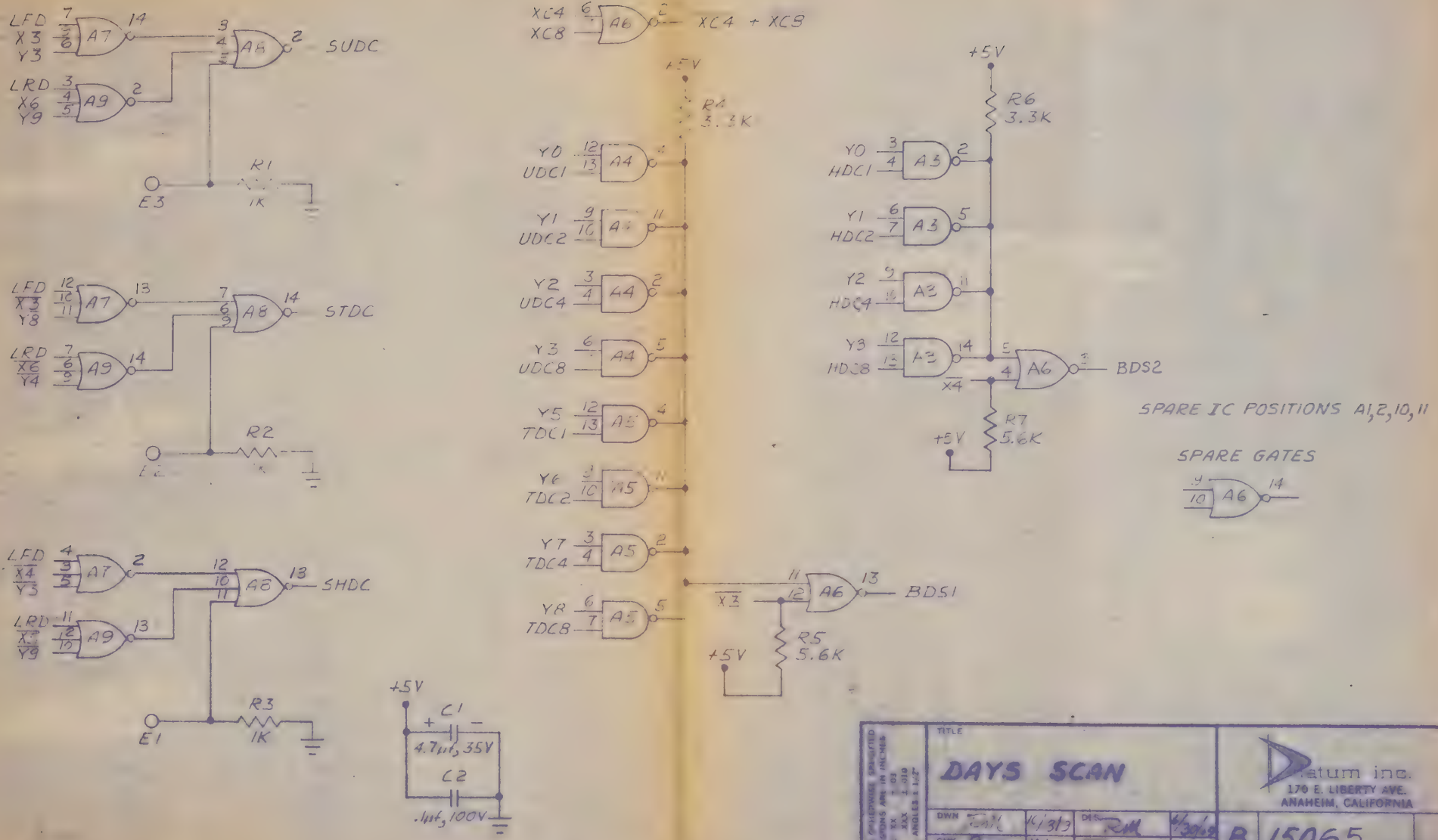
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL XX .03 XXX .010 ANGLES ± 1/2°

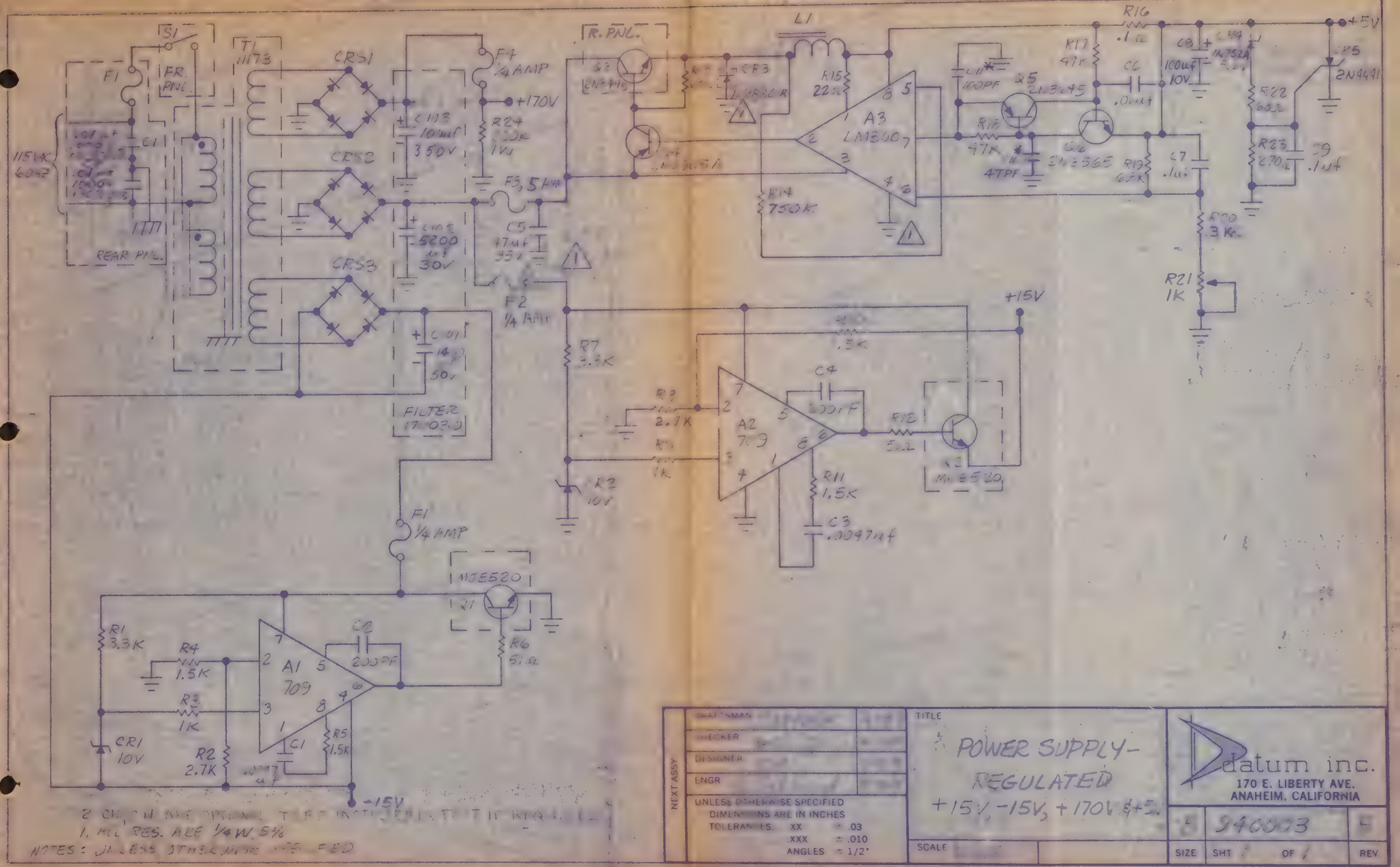
TITLE
PARALLEL OUTPUTS
MS-S-M-H-D

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN MILES	10/13/9	DES		B	15067	A
CHK		ENGR				
SCALE NONE		FSC 31160		SIZE	SHT 2 OF 2	REV

DILTZGEN 19EMC10


LFD
X3
Y3
LRD
X6
Y9
A7
A8
A9
SUDC
E3
R1
1K
LFD
X3
Y8
LRD
X6
Y4
STDC
R2
LFD
X4
Y3
LRD
X7
Y9
SHDC
E1
R3
1K
+5V
C1
4.7µf, 35V
C2
.1µf, 100V
XC4
XC8
XC4 + XC8
R4
3.3K
Y0
UDC1
Y1
UDC2
Y2
UDC4
Y3
UDC8
Y5
TDC1
Y6
TDC2
Y7
TDC4
Y8
TDC8
A4
A5
X3
BDS1
R5
5.6K
R6
3.3K
Y0
HDC1
Y1
HDC2
Y2
HDC4
Y3
HDC8
A3
X4
BDS2
R7
5.6K
SPARE IC POSITIONS A1,2,10,11
SPARE GATES
TITLE
DAYS SCAN
DWN
CHK
SCALE
DES
ENGR
APP
11160
Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
B
15065
SHT 1 OF 1



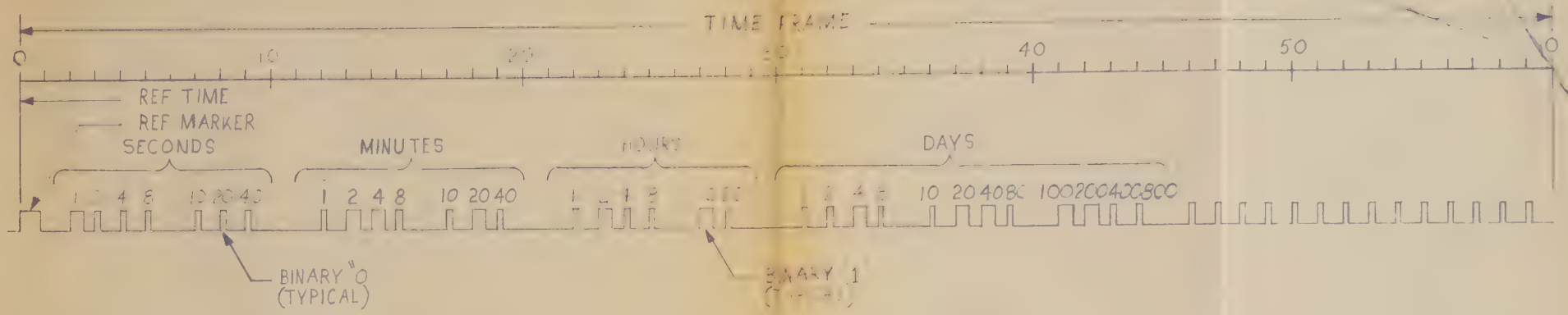
2 CHIPS ARE OPTIONAL THEY INTERCHANGEABLE WITH EACH OTHER

1. ALL RES. ARE 1/4W 5%

NOTES: UNLESS OTHERWISE NOTED

DRAFTSMAN		TITLE	datum inc.
CHECKER		POWER SUPPLY- REGULATED +15V, -15V, +170V & +5V	170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA
DESIGNER			
ENGR			
NEXT ASSY	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES XX ± .03, XXX ± .010, ANGLES ± 1/2°	SCALE	SIZE 940073 REV SHT OF

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



CODE	PULSE RATE	FRAME PERIOD	BINARY ZERO	BINARY ONE	FRAME REFERENCE PULSE	PULSES PER FRAME PERIOD
1	50 PPS	1 SEC	4 MS	10 MS	18 MS	37
2	10 PPS	5 SEC	20 MS	50 MS	90 MS	37
3	5 PPS	10 SEC	40 MS	100 MS	180 MS	37
4	1 PPS	60 SEC	200 MS	500 MS	900 MS	47
5	1 PPS	10 MIN	2 SEC	5 SEC	9 SEC	47

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE: TIMING DIAGRAM SLO CODE (WITH DAYS)

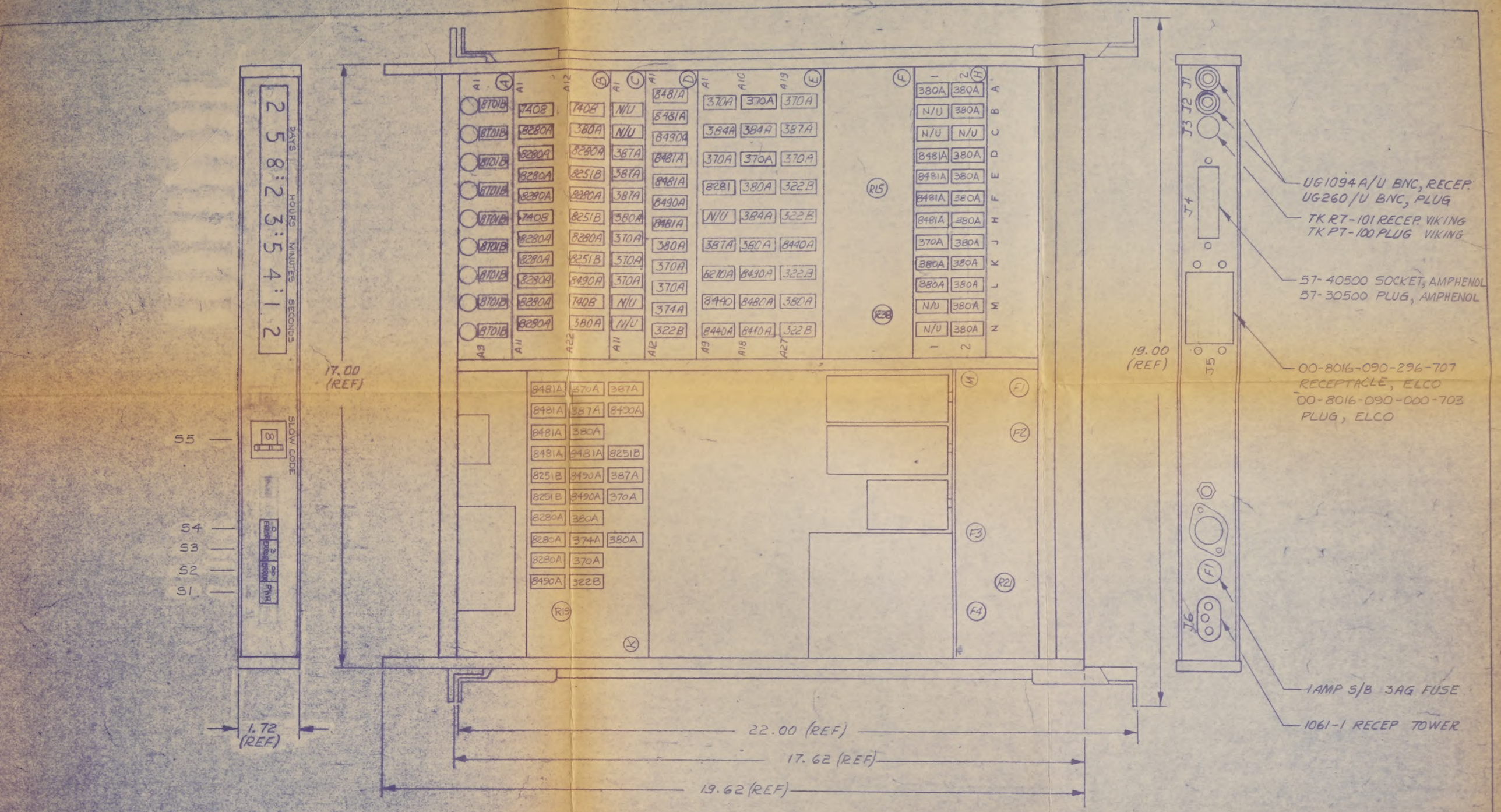
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	AM	12-26-69	DES	
CHK			ENGR	
SCALE	NONE		FSC	31160

B 9100-7000

SIZE SHT 1 OF 1 REV

DIETZGEN 196MG 10



3. SLIDES & REAR MTG BRKTS NOT INCLUDED
2. TOP COVER REMOVED FOR CLARITY
   - (M) 940003 POWER SUPPLY
   - (K) 15068 SLOW CODE
   - (H) 15067 PARALLEL OUTPUTS
   - (F) 15005 AGC AMPL
   - (E) 15033 DECODER
   - (D) 15066 IRIG B ENCODER (DAYS)
   - (C) 15065 DAYS SCAN
   - (B) 15064 TCT/G BASIC - DAYS
   - (A) 15024 DISPLAY ASSY.

1. NOTES:

6. WIRE LIST NO. 800185
5. WIRING DIAGRAM NO.
   - J6- AC POWER INPUT
   - J5- PARALLEL OUTPUTS
   - J4-
   - J3- PULSE RATES
   - J2- SLOW CODE
4. J1 - IRIG B INPUT

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ± .03, XXX ± .010, ANGLES ± 1/2°

TITLE: TIME CODE READER

DWN	MILES	9/11/69	DES	MILES	10/11/69
CHK		11/10	ENGR		11/10
SCALE			FSC	31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE		SHT		OF		REV
C	9200-602		1		1	A

MP MASTER
MA31926